**IN THE CLAIMS**

Please amend the claims as follows:

1. (Currently Amended) An encoder, comprising:

a constellation generator, responsive to an input bitstream to produce an impulse comprising an in-phase component and a quadrature component, said impulse defining symbols within a constellation of symbols;

a pair of vector arithmetic structures (VAS), each VAS adapting a respective one of said in-phase and quadrature components to produce respective shaped in-phase and quadrature components, wherein each VAS comprises:

a plurality of vector registers (VR) for storing precomputed pulse shaping values; and

a vector arithmetic unit (VAU) for arithmetically processing a selected vector and an accumulated vector, said selected vector comprising a plurality of pre-computed values selected from said vector registers in response to a received component signal; and

a combiner, for combining said shaped in-phase and quadrature components to produce an encoded bitstream.

2. (Cancelled)

3. (Currently Amended) The encoder of claim [[2]] 1, wherein said output vector produced by said VAU is stored in an output buffer.

4. (Original) The encoder of claim 3, wherein said output vector produced by said VAU is stored in a vector accumulator (VA) for subsequent arithmetic processing.

5. (Original) The encoder of claim 4, wherein said VAU performs an addition operation in response to said received component signal having a most significant bit (MSB) of a first state, and a subtraction operation in response to said received component signal having a MSB of a second state.

6. (Original) The encoder of claim 1, wherein said constellation of symbols comprise carrierless amplitude and phase (CAP) symbols.

7. (Original) The encoder of claim 1, wherein said constellation of symbols comprise quadrature amplitude modulation (QAM) encoded symbols.

8. (Original) The encoder of claim 1, wherein each VAS processes a received component signal in a manner avoiding a multiplication operation.

9. (Original) The encoder of claim 1, wherein each VAS processes a received component signal in a manner implementing a filtering operation.

10. (Currently Amended) [[A]] An encoding method, comprising:

processing an input bitstream to produce an impulse defining symbols within a constellation of symbols, wherein said impulse comprises an in-phase component and a quadrature component; and

shaping, using a respective vector arithmetic ~~structure (VAS)~~ structures, said in-phase component and said quadrature component to produce a respective shaped ~~component,~~ in-phase and quadrature components;

wherein said shaping comprises arithmetically processing a precomputed vector and an accumulated vector in response to receiving said respective component, said precomputed vectors being selected to impart a desired shape to said respective component.

11. (Cancelled)

12. (Currently Amended) The method of claim [[11]] 10, wherein said arithmetically processed component is added to a vector accumulator for subsequent arithmetic processing.

13. (Original) The method of claim 12, wherein said arithmetic processing comprises an addition operation in response to said received component having a most significant bit (MSB) of a first state, and a subtraction operation in response to said received component having an MSB of a second state.

14. (Original) The method of claim 10, wherein said constellation of symbols comprises pulse code modulated (PCM) symbols.

15. (Cancelled)

16. (Original) The method of claim 15, further comprising the step of:

combining said shaped in-phase and quadrature components to produce an encoded bitstream.